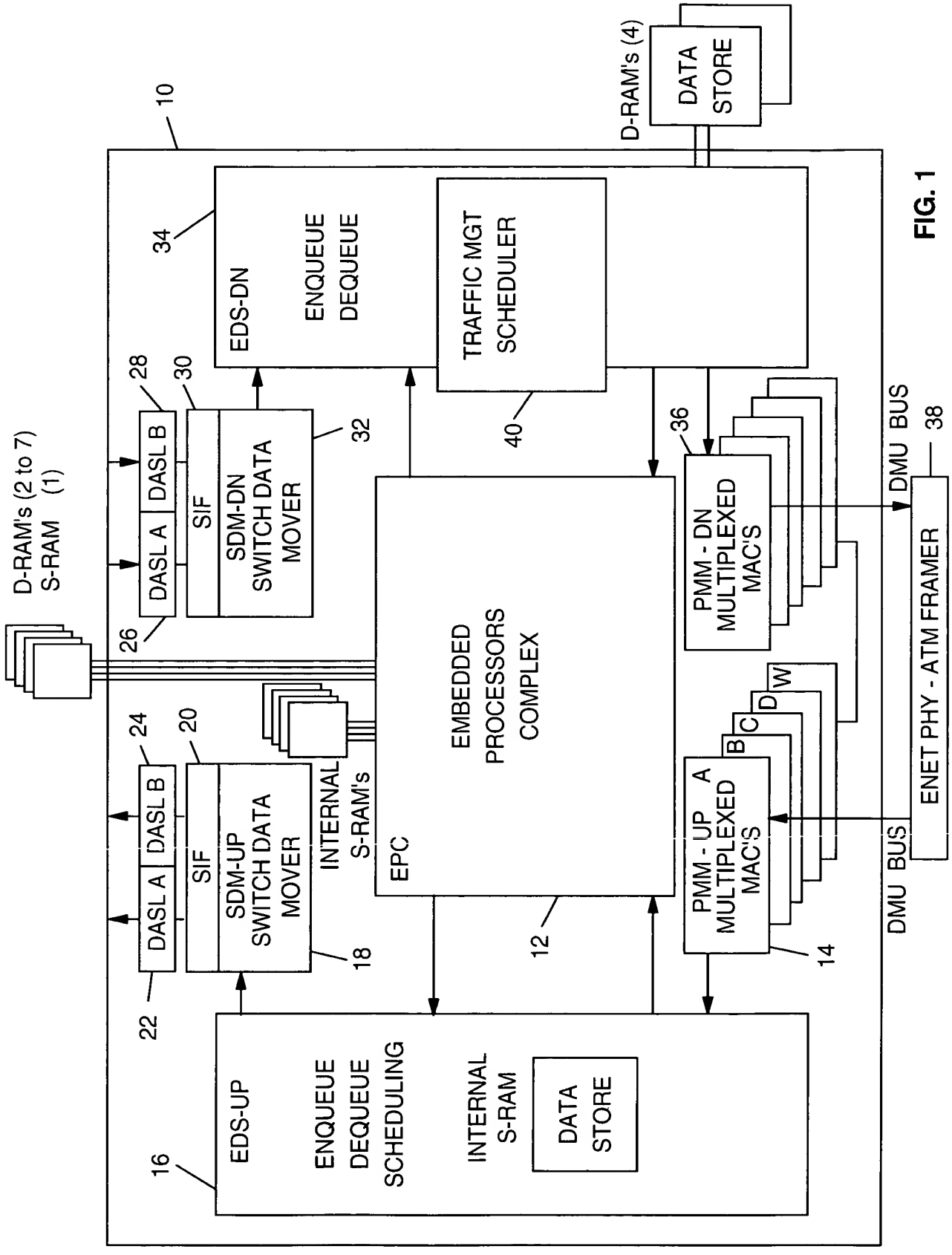

10
D-RAM's (4)
DATA STORE
34
EDS-DN
ENQUEUE
DEQUEUE
TRAFFIC MGT SCHEDULER
40
28
30
DASL B
DASL A
SIF
SDM-DN SWITCH DATA MOVER
32
D-RAM's (2 to 7)
S-RAM (1)
26
36
PMM - DN MULTIPLEXED MAC'S
DMU BUS
38
ENET PHY - ATM FRAMER
EMBEDDED PROCESSORS COMPLEX
24
20
DASL B
DASL A
SIF
SDM-UP SWITCH DATA MOVER
INTERNAL S-RAM's
EPC
12
B
C
D
W
PMM - UP A MULTIPLEXED MAC'S
18
14
DMU BUS
22
16
EDS-UP
ENQUEUE
DEQUEUE
SCHEDULING
INTERNAL S-RAM
DATA STORE

FIG. 1

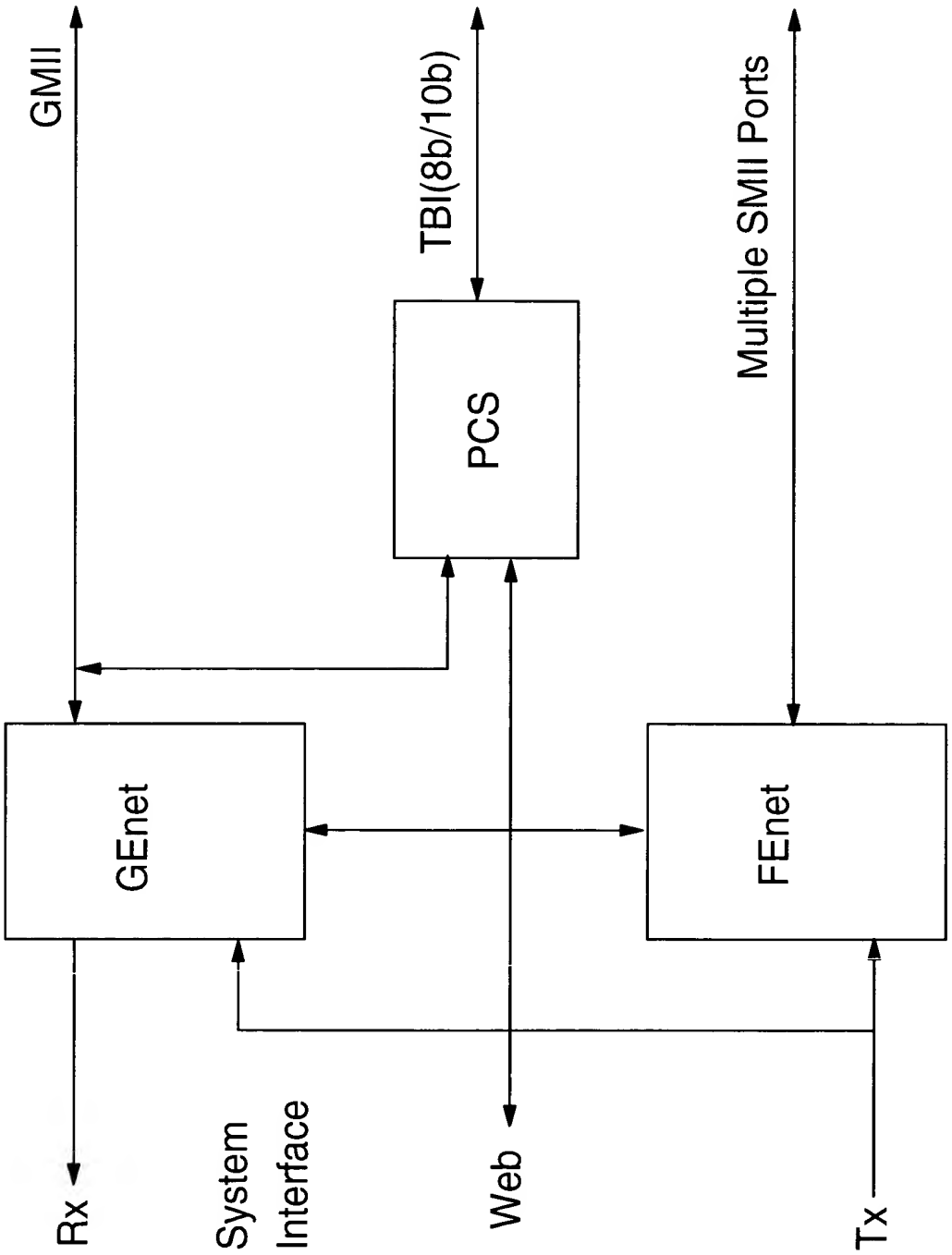

GMII
TBI(8b/10b)
Multiple SMII Ports
PCS
GEnet
FEnet
Rx
System Interface
Web
Tx

FIG. 1A

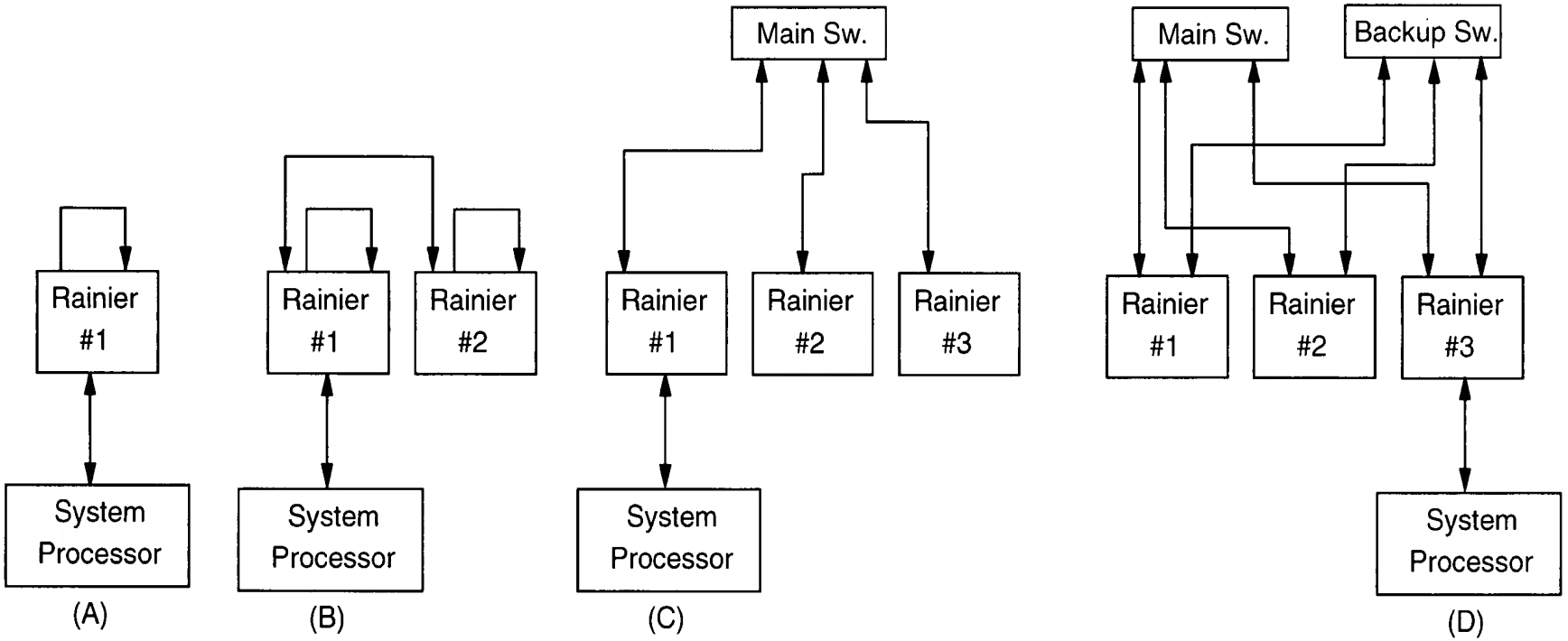


FIG. 2 System Configurations

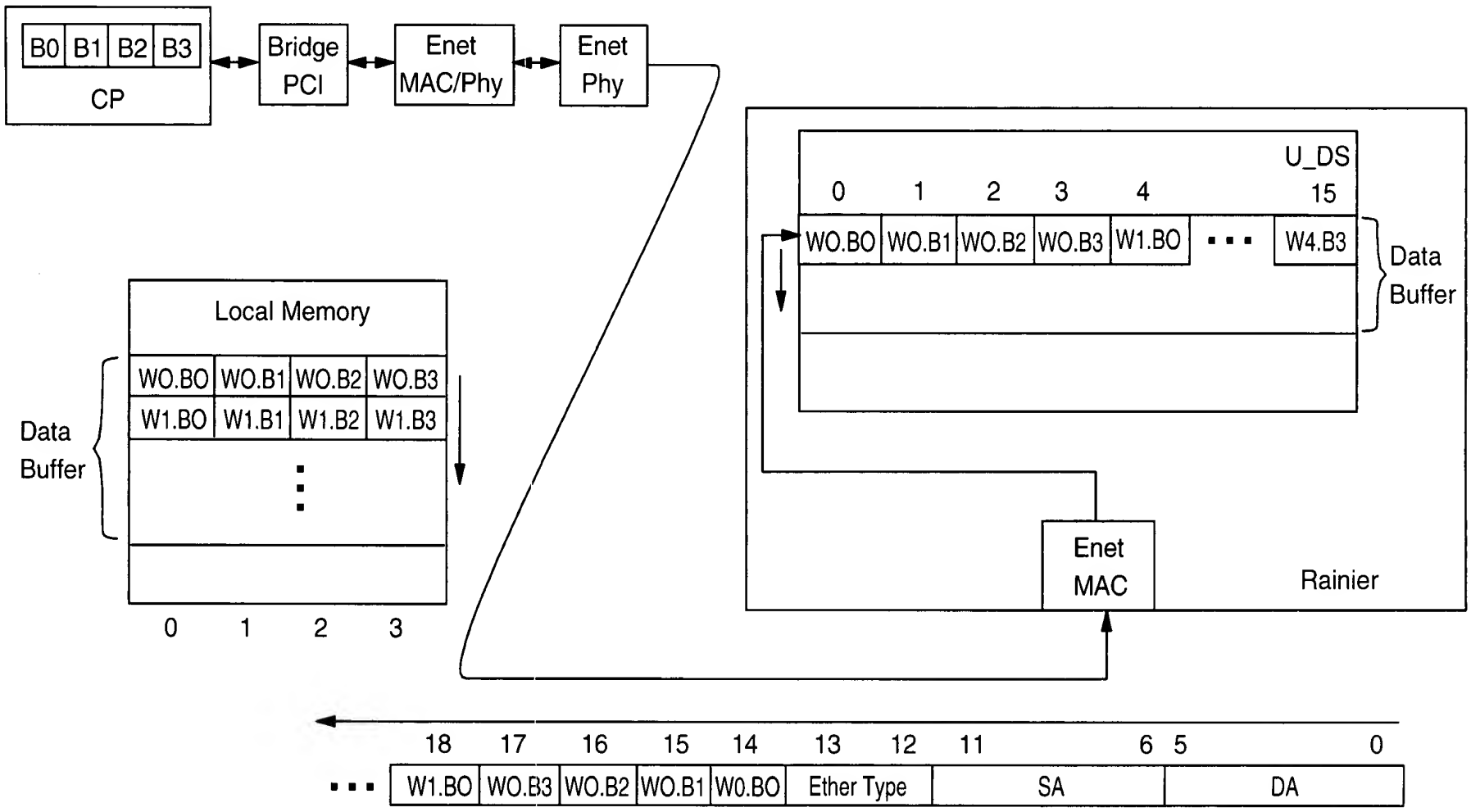


FIG. 3 Guided Traffic Data Flow (Ethernet Port)

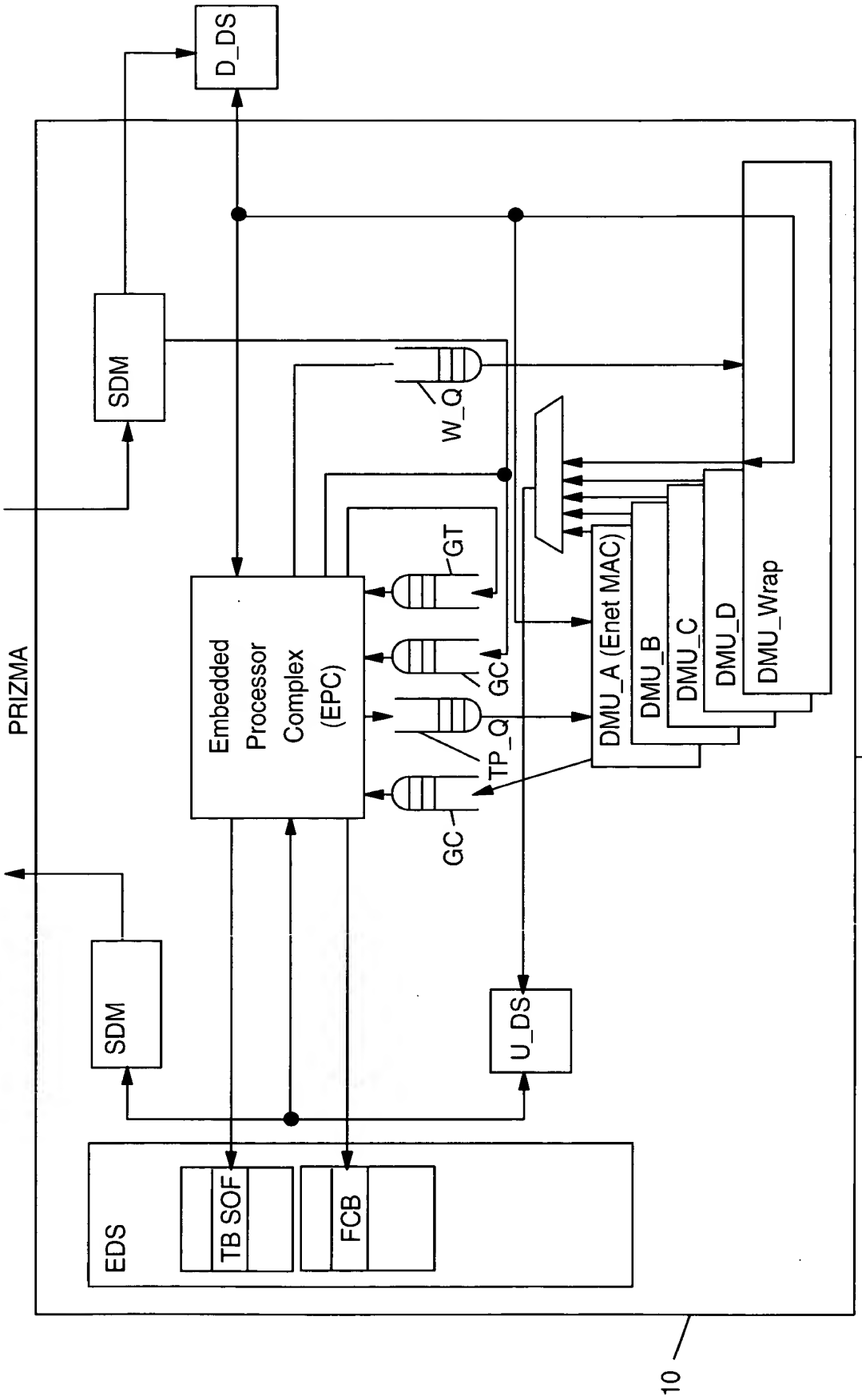


FIG. 4 Flow of Guided Traffic

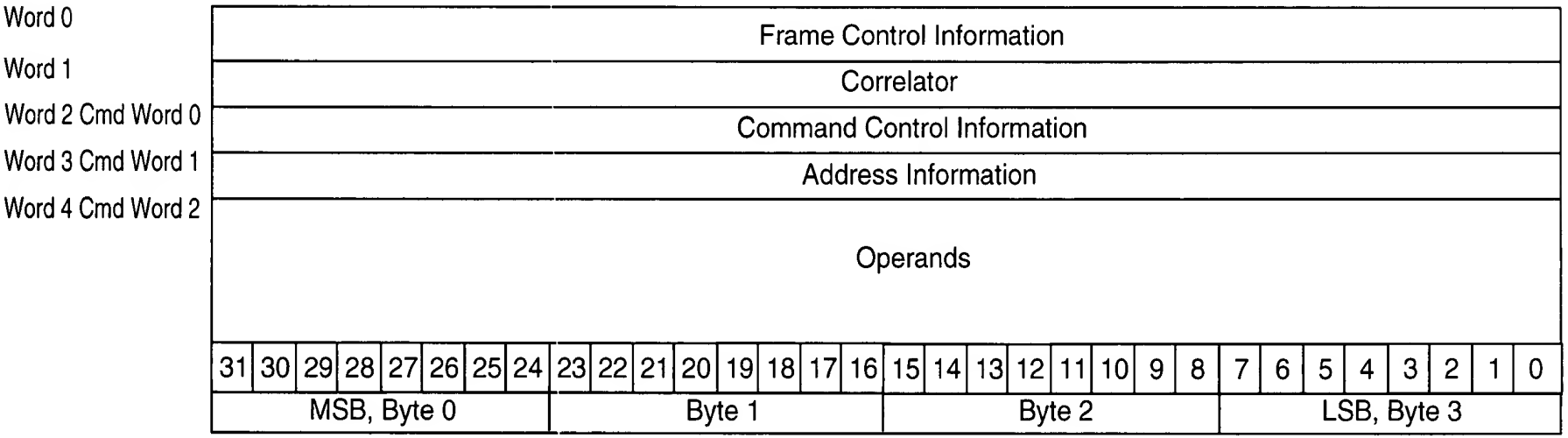


FIG. 5

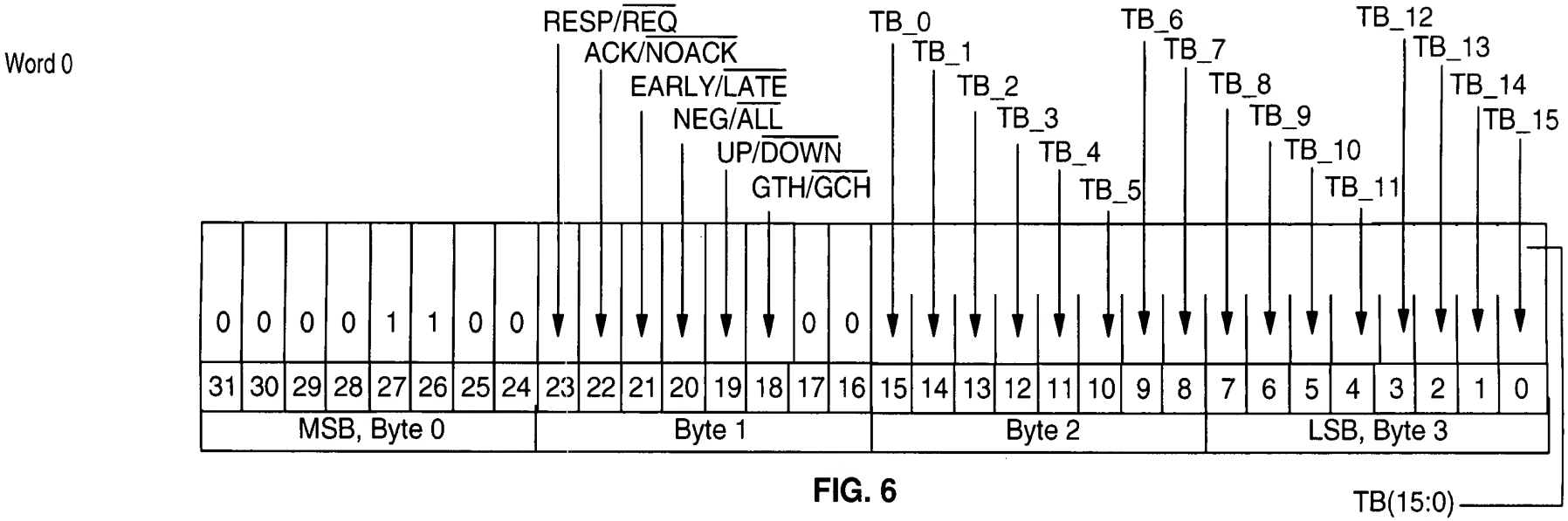


FIG. 6

Word 1

Correlator																											
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSB, Byte 0								Byte 1								Byte 2								LSB, Byte 3							

FIG. 7 Correlator

Word 2 Cmd Word 0

1	L															Completion Code								res				GC Type			
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSB, Byte 0								Byte 1								Byte 2								LSB, Byte 3							

FIG. 8 Command Control Information Format

Word 3 Cmd Word 1

Address																											
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSB, Byte 0								Byte 1								Byte 2								LSB, Byte 3							

FIG. 9 Addressing Information Format

Island ID	Structure Address	Element Address	Word Addr
5	23		4
32			

FIG. 10 General Form of Structure Addressing

Island_ID	Island Name
'00000'b	UpData Store*
'00001'b	Up PMM
'00010'b	Up EDS
'00011'b	Up SDM
'00100'b	Embedded PRocessor Complex
'00101'b	SPM
'00110-00111'b	reserved
'01000'b	Control Memories*
'01001-01111'b	reserved
'10000'b	Down Data Store*
'10001'b	Down PMM
'10010'b	Down EDS
'10011'b	Down SDM
'10100'b	Configuration Registers
'10101'b	DASL
'10110-11111'b	reserved
*These islands are not accessible via the Web interface	

FIG. 11 Addressing, Island Encoding

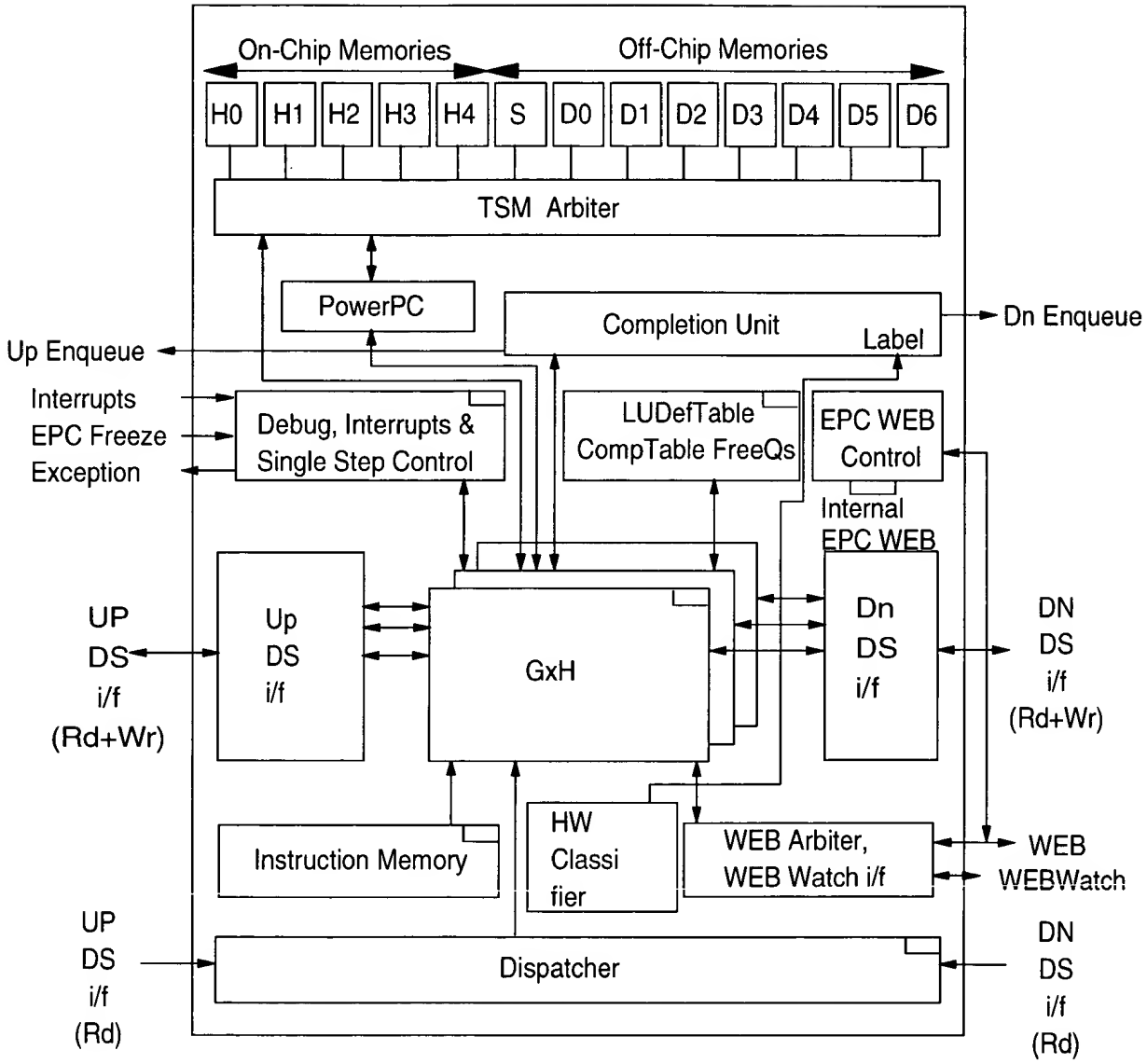


FIG. 12A BLOCK GIAGRAM OF THE EPC

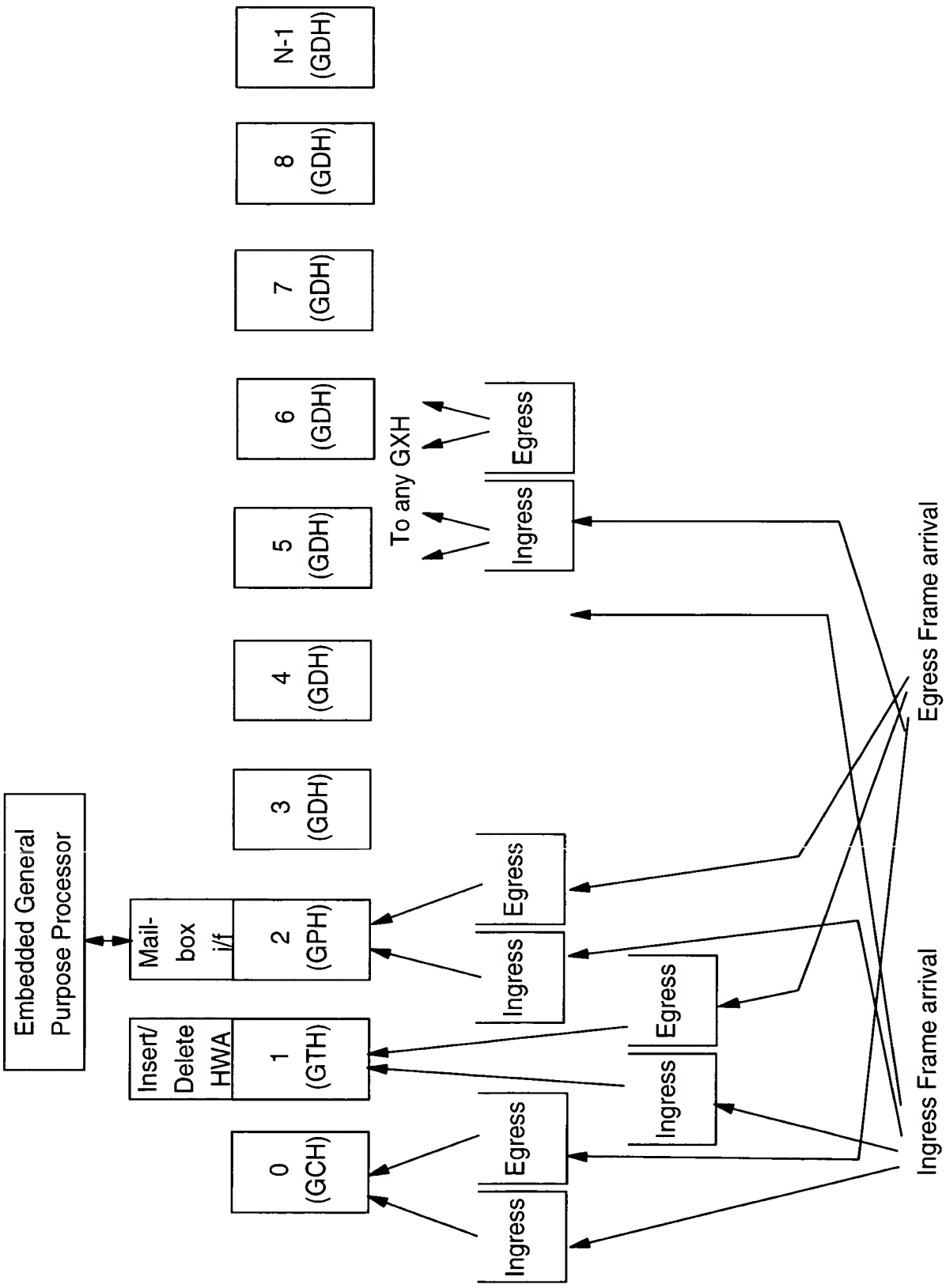


FIG. 12B The 10 GxHs

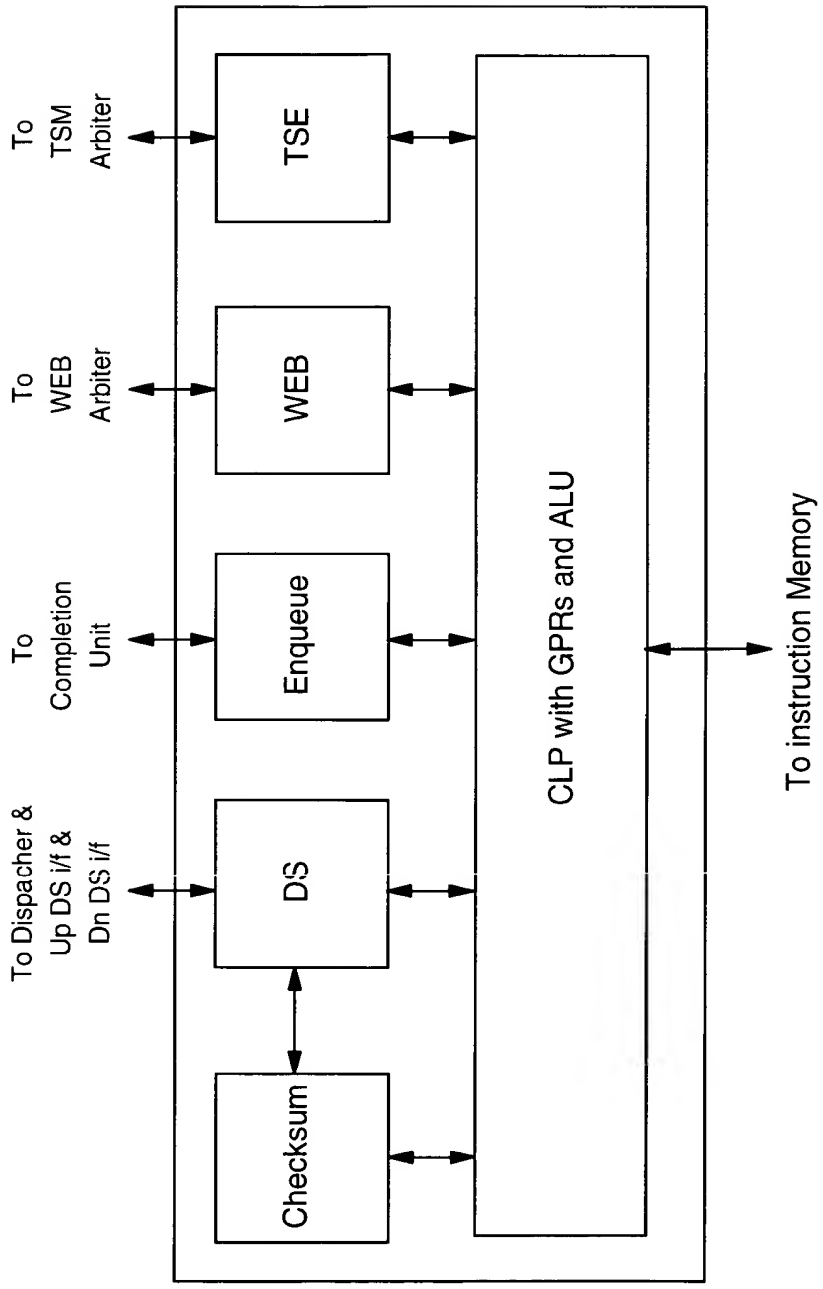

To Dispacher & Up DS i/f & Dn DS i/f
To Completion Unit
To WEB Arbiter
To TSM Arbiter
Checksum
DS
Enqueue
WEB
TSE
CLP with GPRs and ALU
To instruction Memory

FIG. 12C

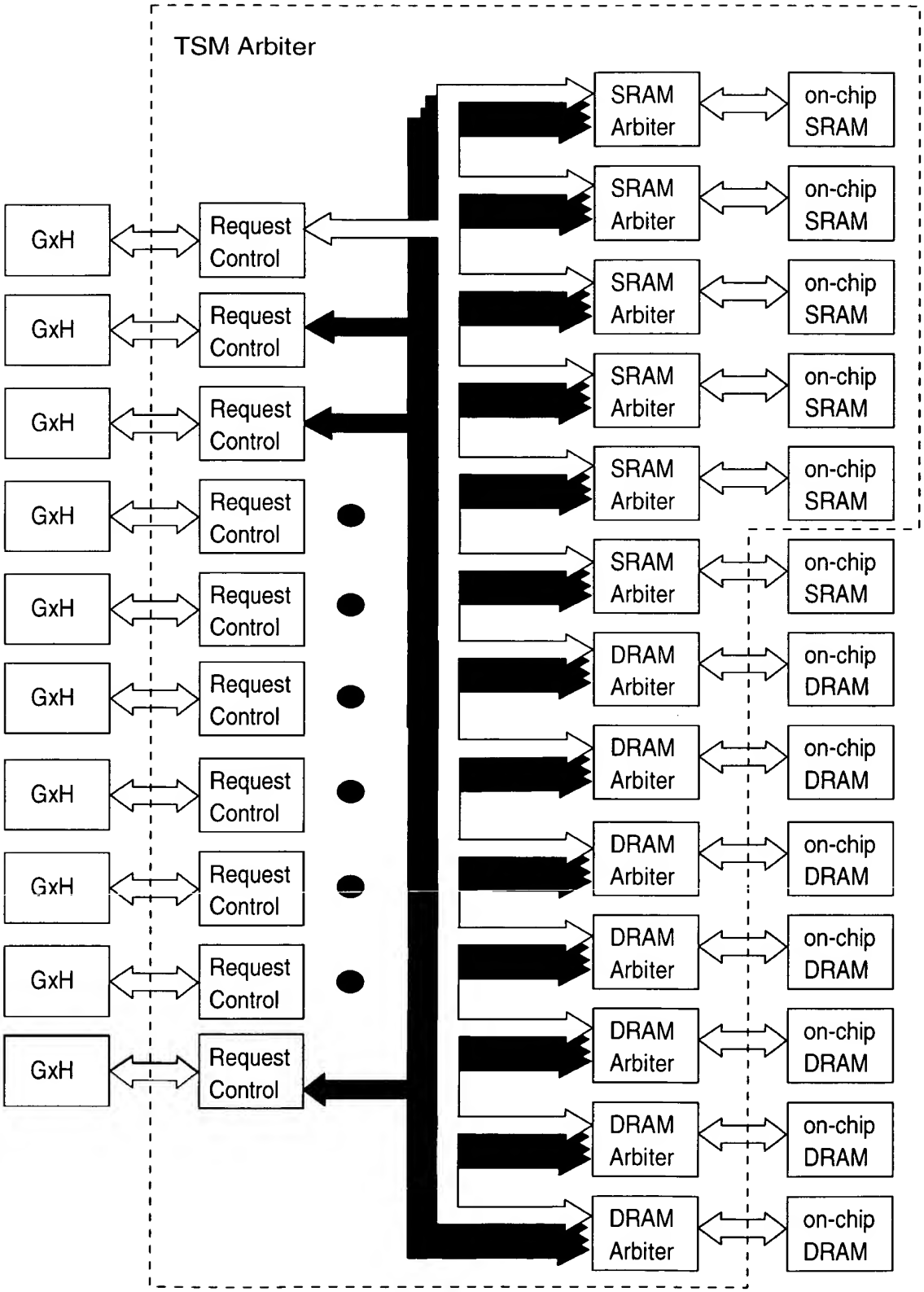


FIG. 13 (Memory Complex)

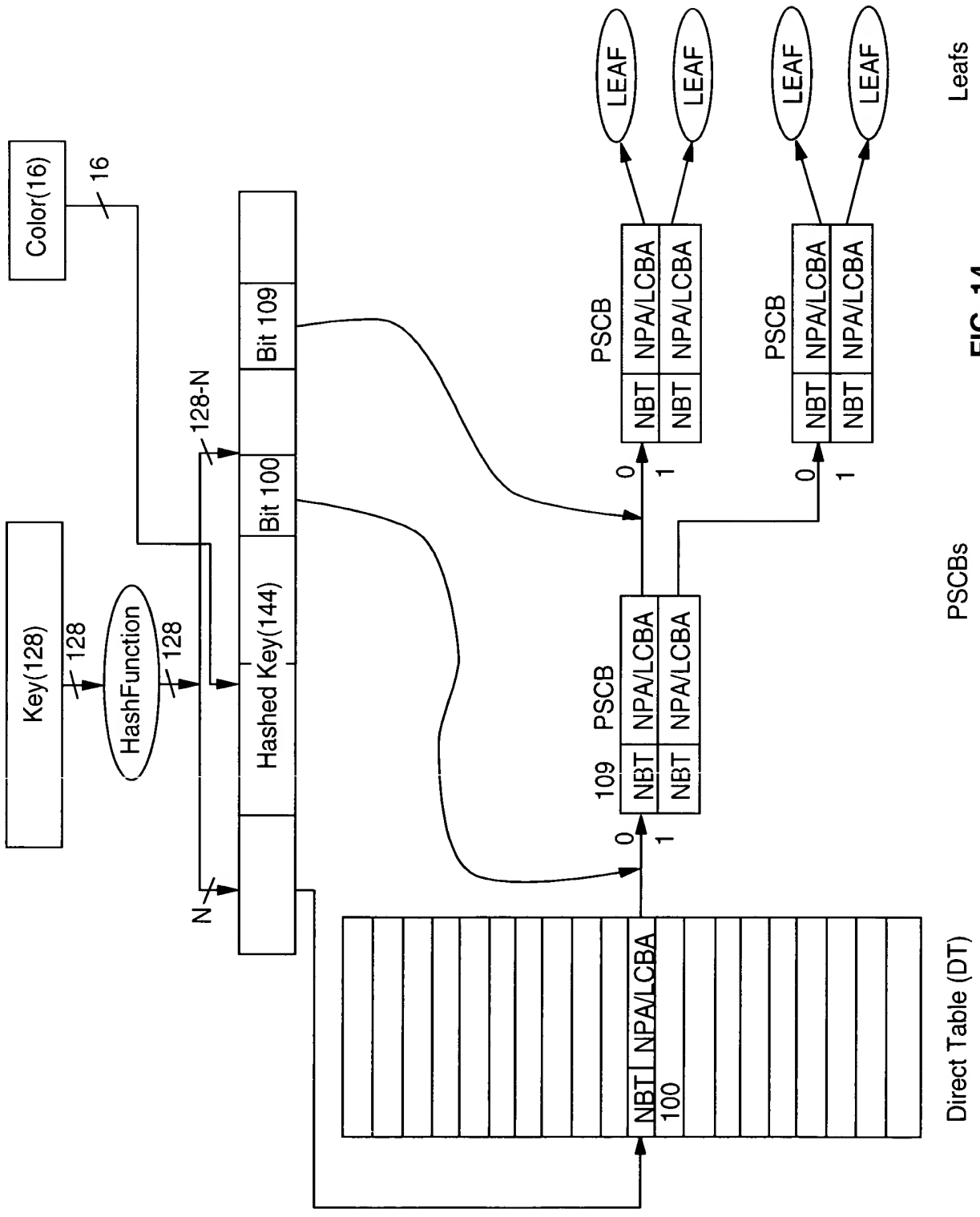
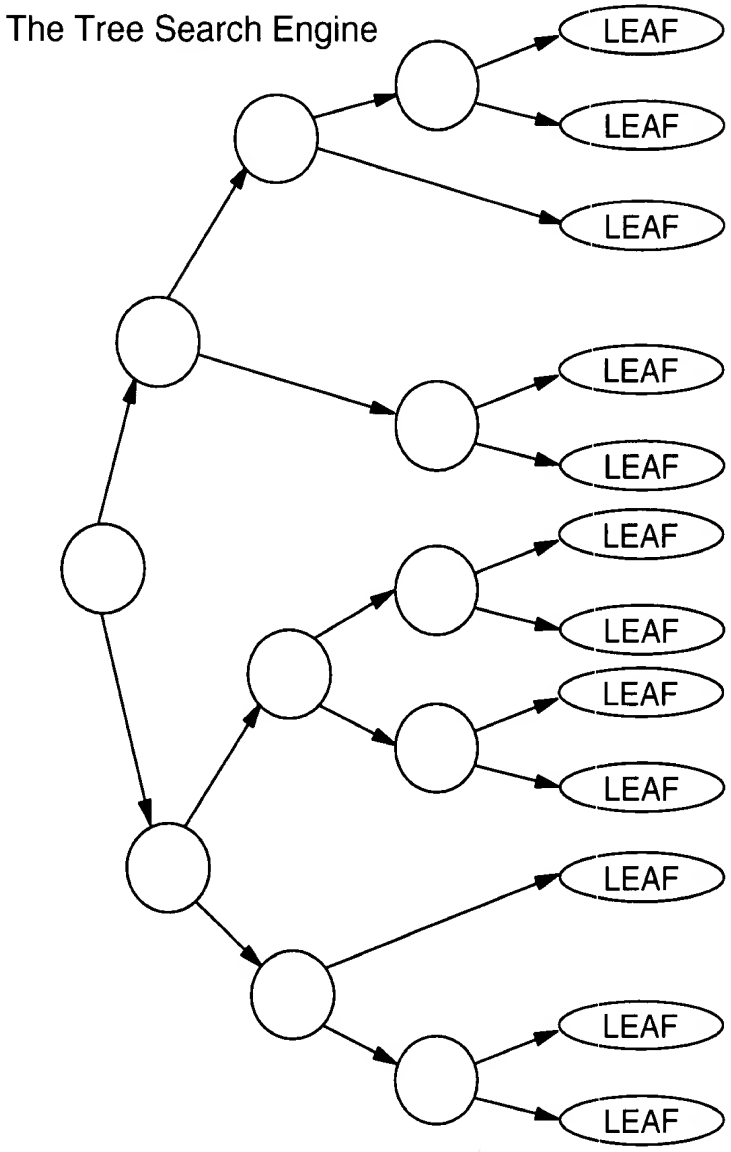
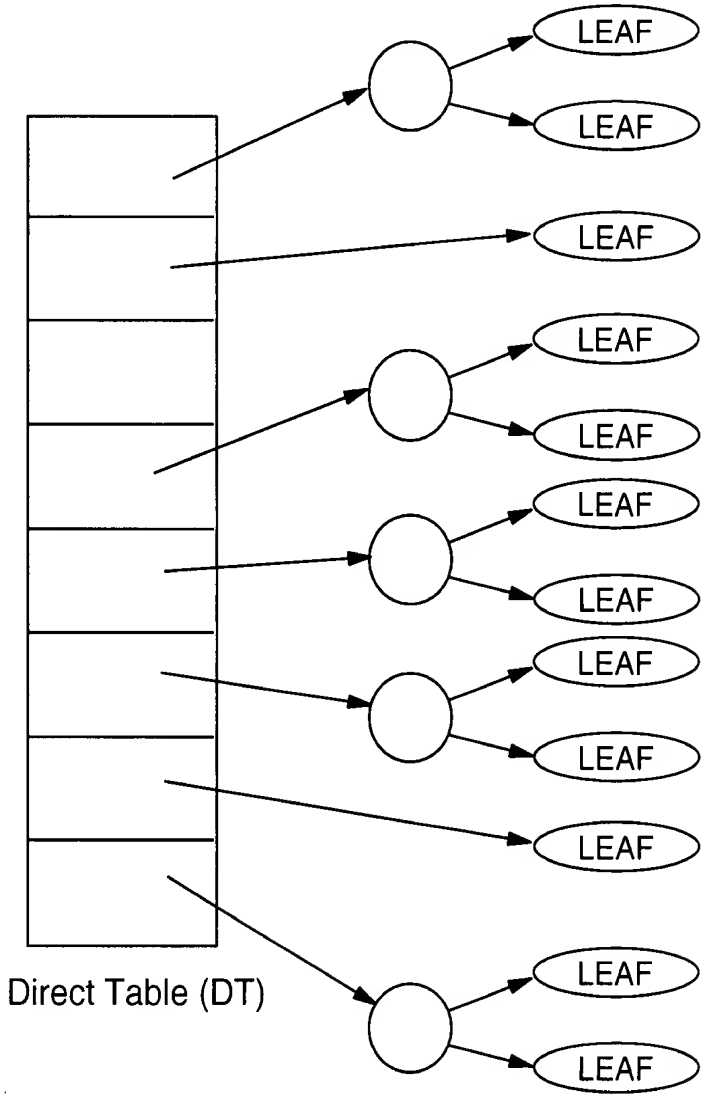

Color(16)
16
Key(128)
128
HashFunction
128
Hashed Key(144)
128-N
N
Bit 109
Bit 100
PSCB
NBT
NPA/LCBA
109
100
0
1
LEAF
Direct Table (DT)
PSCBs
Leafs

FIG. 14



Datastructure without using a Direct Table



Datastructure with using a Direct Table

FIG. 15

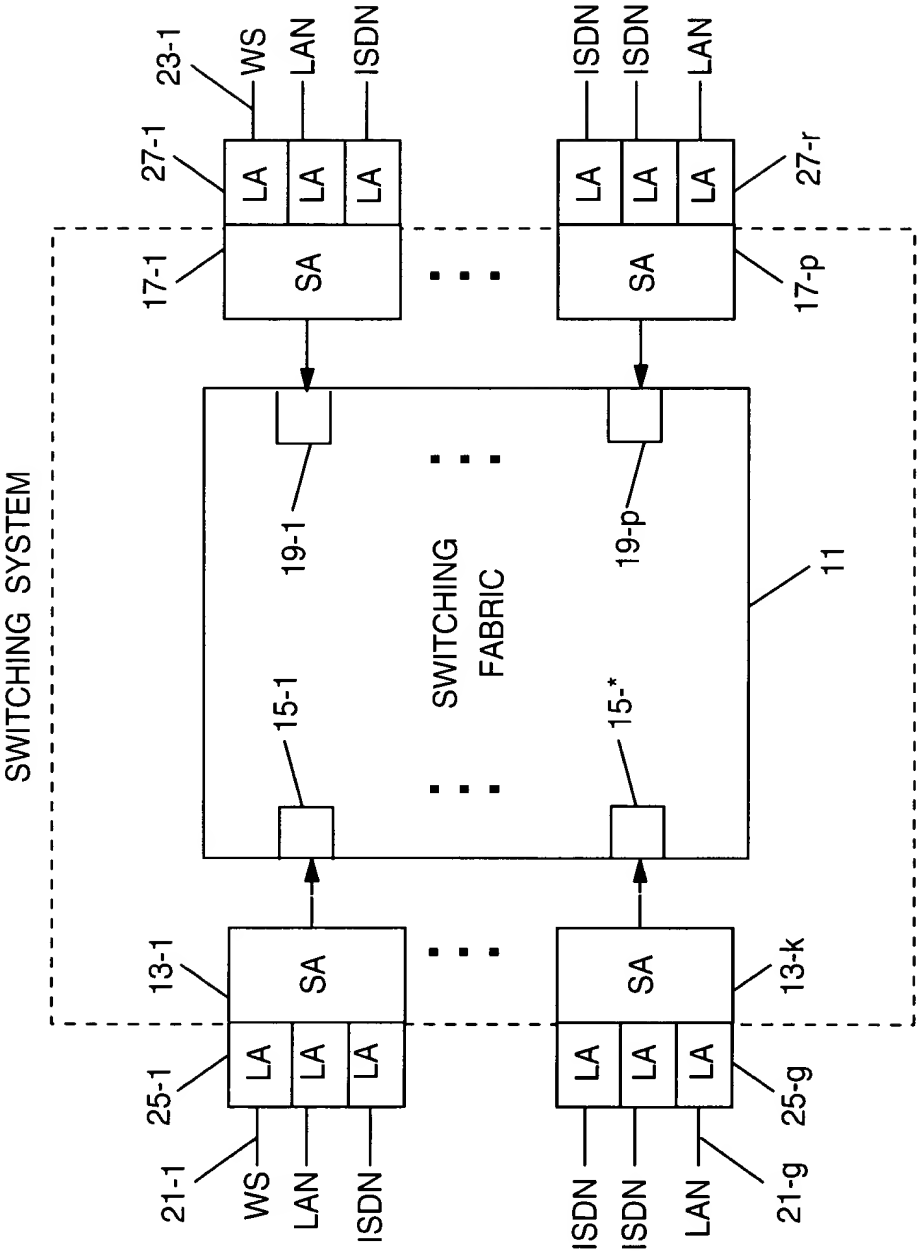

SWITCHING SYSTEM
SWITCHING FABRIC
11
13-1
13-k
SA
SA
LA
LA
LA
25-1
25-g
21-1
21-g
WS
LAN
ISDN
ISDN
ISDN
LAN
15-1
15-*
19-1
19-p
17-1
17-p
27-1
27-r
23-1
WS
LAN
ISDN
ISDN
ISDN
LAN

FIG. 16

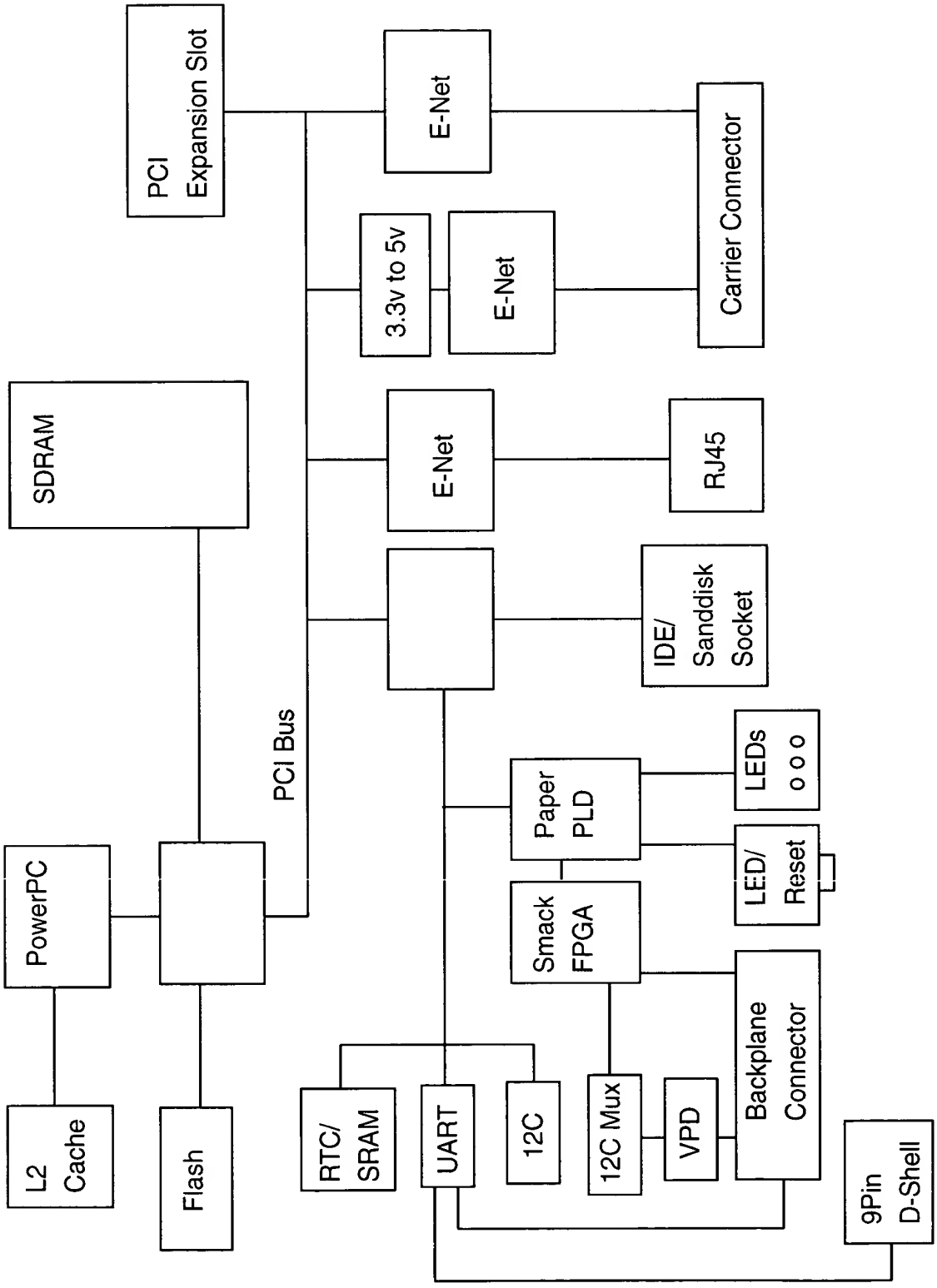

PCI Expansion Slot
E-Net
Carrier Connector
3.3v to 5v
E-Net
SDRAM
E-Net
RJ45
IDE/ Sanddisk Socket
PCI Bus
PowerPC
Paper PLD
LEDs o o o
LED/ Reset
Smack FPGA
Backplane Connector
L2 Cache
Flash
RTC/ SRAM
UART
12C
12C Mux
VPD
9Pin D-Shell

FIG. 17

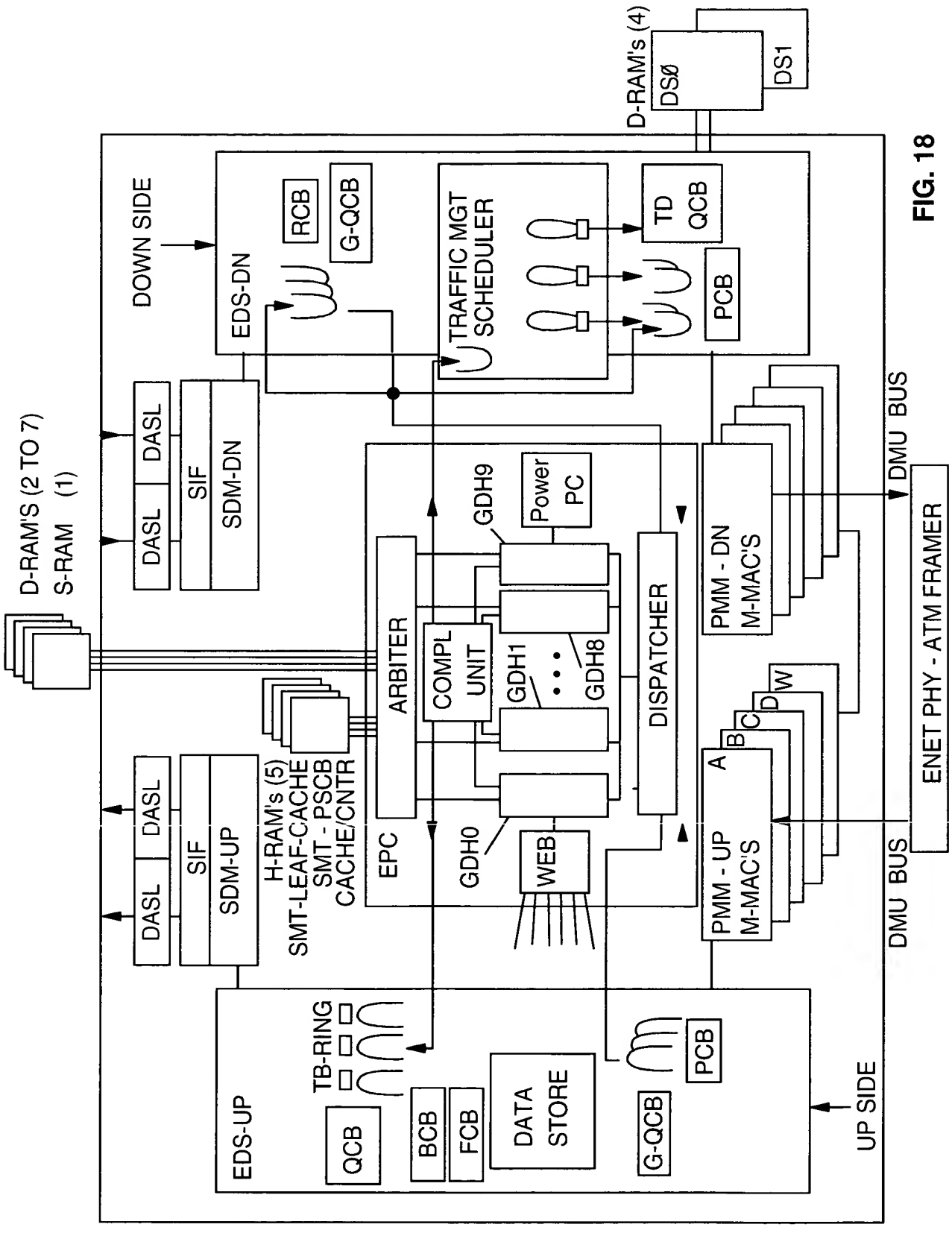

D-RAM'S (2 TO 7)
S-RAM (1)
DOWN SIDE
EDS-DN
RCB
G-QCB
TRAFFIC MGT SCHEDULER
TD QCB
PCB
D-RAM's (4)
DSØ
DS1
DASL
SIF
SDM-DN
ARBITER
COMPL UNIT
GDH9
Power PC
GDH1
GDH8
GDH0
WEB
EPC
DISPATCHER
PMM - DN M-MAC'S
DMU BUS
ENET PHY - ATM FRAMER
H-RAM's (5)
SMT-LEAF-CACHE
SMT - PSCB
CACHE/CNTR
SDM-UP
PMM - UP M-MAC'S
A
B
C
D
W
EDS-UP
TB-RING
QCB
BCB
FCB
DATA STORE
G-QCB
PCB
UP SIDE

FIG. 18